

<b>Chapter 1 : Introduction to VLSI</b>	<b>1-1 to 1-6</b>	2.5.4 Measurement of Parameters ..... 2-14
1.1 Historical Perspective ..... 1-1		<b>2.6 Channel Length Modulation ..... 2-16</b>
1.1.1 Comparison of NMOS and CMOS Technology ..... 1-3		<b>2.7 Body Bias Effect ..... 2-17</b>
1.2 Abstraction Levels in Digital Circuits ... 1-3		<b>2.8 Scaling and Small Geometry Effect ..... 2-19</b>
1.3 Concepts of Regularity, Modularity and Locality ..... 1-4		2.8.1 Full Scaling (Constant Field Scaling) ..... 2-19
1.4 VLSI Design Flow - Y- Chart Representation ..... 1-4		2.8.2 Constant Voltage Scaling ..... 2-20
		2.8.3 Limitations of Scaling ..... 2-21
<b>Chapter 2 : Review of MOSFET Operation and Fabrication</b>	<b>2-1 to 2-85</b>	<b>2.9 Short Channel Effects ..... 2-21</b>
2.1 Basic MOSFET Structure ..... 2-1		2.9.1 Sub-threshold Conduction ..... 2-23
2.1.1 Enhancement Type MOSFET ..... 2-1		<b>2.10 Drain Induced Barrier Lowering and Punch Through ..... 2-23</b>
2.1.1.1 nMOS Transistor ..... 2-1		2.11 Velocity Saturation ..... 2-24
2.1.1.2 pMOS Transistor ..... 2-2		<b>2.12 Hot Electron Effect ..... 2-24</b>
2.1.1.3 Advantages of nMOSFET over pMOSFET ..... 2-3		2.12.1 Prevention Techniques ..... 2-25
2.1.2 Depletion Type MOSFET ..... 2-3		<b>2.13 FET Capacitances ..... 2-25</b>
2.1.2.1 n-Channel Depletion Type MOSFET ..... 2-3		<b>2.14 Solved Problems ..... 2-28</b>
2.1.2.2 p-Channel Depletion Type MOSFET ..... 2-4		<b>2.15 Latch Up ..... 2-30</b>
2.2 MOSFET Operation ..... 2-4		<b>2.16 MOSFET Modeling Using SPICE ..... 2-31</b>
2.3 n-Channel Depletion Type MOSFET Operation ..... 2-7		<b>2.17 Fabrication Processes ..... 2-33</b>
2.4 p-Channel Depletion Type MOSFET Operation ..... 2-8		2.17.1 Oxidation ..... 2-33
2.5 Derivation of V-I Relationship for Enhancement Type n-MOSFET ..... 2-9		2.17.2 Diffusion ..... 2-33
2.5.1 Non Saturated Region ..... 2-9		2.17.3 Ion Implantation ..... 2-33
2.5.1.1 Saturated Region ..... 2-10		2.17.4 Epitaxy ..... 2-34
2.5.2 Channel Length Modulation ..... 2-12		2.17.5 Metallization ..... 2-34
2.5.3 Body Bias Effect ..... 2-13		<b>2.18 Lithography ..... 2-35</b>
		2.18.1 Photoresist ..... 2-35
		<b>2.19 Mask Generation ..... 2-36</b>
		<b>2.20 Process to Pattern SiO<sub>2</sub> ..... 2-38</b>
		<b>2.21 NMOS Transistor Fabrication ..... 2-38</b>
		<b>2.22 PMOS Transistor Fabrication ..... 2-41</b>
		<b>2.23 LOCOS Technique ..... 2-44</b>
		<b>2.24 Complementary MOS (CMOS) ..... 2-45</b>

<b>2.25</b>	<b>CMOS n-well Process.....</b>	<b>2-46</b>	<b>Chapter 3 : Combinational CMOS Logic Circuit</b>	
<b>2.26</b>	<b>CMOS p-well Process.....</b>	<b>2-50</b>	<b>3-1 to 3-36</b>	
<b>2.27</b>	<b>Twin Tub Process.....</b>	<b>2-52</b>	<b>3.1</b>	<b>MOSFET as a Switch.....</b>
<b>2.28</b>	<b>Device Isolation .....</b>	<b>2-57</b>	<b>3.2</b>	<b>MOS Inverters and Voltage Transfer</b>
<b>2.29</b>	<b>Layout Introduction .....</b>	<b>2-58</b>		<b>Characteristics .....</b>
<b>2.30</b>	<b>Stick Diagram .....</b>	<b>2-58</b>	<b>3.2.1</b>	<b>Noise Margin .....</b>
2.30.1	nMOS Circuit Stick Diagram.....	2-59	<b>3.2.2</b>	<b>Resistive Load Inverter.....</b>
2.30.2	CMOS Stick Diagram .....	2-59	<b>3.2.3</b>	<b>Depletion Load Inverter</b>
<b>2.31</b>	<b>Design Rules .....</b>	<b>2-61</b>		(HMOS - High Performance MOS) .....
2.31.1	Need of Design Rules.....	2-62	<b>3.2.4</b>	<b>3-6</b>
2.31.1.1	Micron Rule.....	2-62	<b>3.2.5</b>	<b>Pseudo - nMOS Logic .....</b>
2.31.1.2	Lambda Rule.....	2-62	<b>3.2.6</b>	<b>3-8</b>
<b>2.32</b>	<b>CMOS Design Rules .....</b>	<b>2-63</b>	<b>3.3</b>	<b>CMOS Inverter .....</b>
<b>2.33</b>	<b>CMOS Inverter Layout .....</b>	<b>2-65</b>		<b>3-9</b>
<b>2.34</b>	<b>CMOS NAND and NOR Gate Layout.....</b>	<b>2-67</b>	<b>3.4</b>	<b>DC Characteristics of the CMOS</b>
<b>2.35</b>	<b>nMOS Design Rules.....</b>	<b>2-69</b>		<b>Inverter.....</b>
2.35.1	Interlayer Contacts .....	2-72	<b>3.5</b>	<b>3-9</b>
2.35.1.1	Butting Contact.....	2-72		<b>CMOS Inverter Switching</b>
2.35.1.2	Burried Contact.....	2-73		<b>Characteristics .....</b>
<b>2.36</b>	<b>nMOS Depletion Load Inverter.....</b>	<b>2-73</b>	<b>3.5.1</b>	<b>3-14</b>
<b>2.37</b>	<b>nMOS 2-input NAND Gate .....</b>	<b>2-75</b>	<b>3.5.2</b>	<b>Combinational Logic Design using</b>
<b>2.38</b>	<b>Use of CAD Tools for Layout and</b>		<b>3.5.3</b>	<b>Static CMOS Technique .....</b>
	<b>Simulation .....</b>	<b>2-75</b>	<b>3.5.4</b>	<b>3-18</b>
<b>2.39</b>	<b>GaAs Technology .....</b>	<b>2-76</b>	<b>3.6</b>	<b>NAND Gate .....</b>
2.39.1	MESFET Device.....	2-76	<b>3.6.1</b>	<b>3-18</b>
2.39.2	Modulation Doped Field Effect			<b>NOR Gate .....</b>
	Transistor (MODFET).....	2-77	<b>3.5.5</b>	<b>3-19</b>
2.39.3	Optoelectronic Devices .....	2-78		<b>Complex CMOS Logic circuits.....</b>
2.39.3.1	Light Emitting Diode (LED).....	2-78		<b>3-19</b>
<b>2.40</b>	<b>Multigate Devices.....</b>	<b>2-80</b>	<b>3.5.6</b>	<b>Static CMOS Design.....</b>
<b>2.41</b>	<b>Carbon Nano-Tube FET .....</b>	<b>2-83</b>	<b>3.5.7</b>	<b>3-20</b>
			<b>3.6</b>	<b>FET Sizing.....</b>
			<b>3.6.1</b>	<b>3-22</b>
			<b>3.7</b>	<b>2-Input NOR Gate .....</b>
				<b>3-23</b>
			<b>3.8</b>	<b>Solved Problems.....</b>
				<b>3-24</b>
			<b>Chapter 4 : MOS Design Styles</b>	<b>4-1 to 4-37</b>
			<b>4.1</b>	<b>Pass Transistor Logic.....</b>
			<b>4.2</b>	<b>Pseudo - n-MOS .....</b>
			<b>4.3</b>	<b>4-1</b>
			<b>4.4</b>	<b>Static CMOS Design.....</b>
			<b>4.5</b>	<b>4-7</b>
				<b>Dynamic Logic Circuits.....</b>
				<b>4-8</b>
				<b>Dynamic Logic Circuit Structure.....</b>
				<b>4-8</b>



4.5.1	Comparison of Pseudo NMOS, Dynamic Static CMOS Logic.....	4-12	5.3.1	Structure of RAM.....	5-3	
<b>4.6</b>	<b>Race Problem .....</b>	<b>4-12</b>	5.3.2	SRAM Read and Transistor Sizing.....	5-5	
<b>4.7</b>	<b>Domino Logic.....</b>	<b>4-14</b>	5.3.3	SRAM Write and Transistor Sizing .....	5-6	
4.7.1	NORA Logic (No Race) Zipper Logic.....	4-15	5.3.4	SRAM Write Circuitry .....	5-7	
<b>4.8</b>	<b>MODL (Multiple Output Domino Logic).....</b>	<b>4-17</b>	<b>5.4</b>	<b>Sense Amplifier.....</b>	<b>5-8</b>	
<b>4.9</b>	<b>Clocked CMOS (C2 MOS) .....</b>	<b>4-17</b>	<b>5.5</b>	<b>SRAM Memory Cell with Resistive Load .....</b>	<b>5-9</b>	
<b>4.10</b>	<b>Solved Problems.....</b>	<b>4-18</b>	<b>5.6</b>	<b>Dynamic Memory .....</b>	<b>5-10</b>	
<b>4.11</b>	<b>Sequential Circuits .....</b>	<b>4-25</b>	<b>5.7</b>	<b>Three-Transistor DRAM Cell.....</b>	<b>5-11</b>	
<b>4.12</b>	<b>Latches and Flip flops.....</b>	<b>4-25</b>	<b>5.8</b>	<b>Read Only Memories (ROM).....</b>	<b>5-12</b>	
4.12.1	SR Latch .....	4-26	<b>5.9</b>	<b>Mask Programmable ROM .....</b>	<b>5-13</b>	
4.12.2	Clocked SR-Latch.....	4-27	<b>5.10</b>	<b>NOR based ROM Array.....</b>	<b>5-13</b>	
4.12.3	Clocked JK-Latch.....	4-27	<b>5.11</b>	<b>Design of Row and Column Decoders for NOR-based ROM.....</b>	<b>5-15</b>	
4.12.4	D-Latch.....	4-28	<b>5.12</b>	<b>NAND based ROM .....</b>	<b>5-17</b>	
4.12.5	D-Latch with Enable Input.....	4-28	<b>5.13</b>	<b>Row Decoder for a NAND based ROM.....</b>	<b>5-18</b>	
<b>4.13</b>	<b>Static CMOS D-Latch .....</b>	<b>4-28</b>	<b>5.14</b>	<b>EPROM (Erasable Programmable Read Only Memory) .....</b>	<b>5-18</b>	
4.13.1	Pseudo Static CMOS D-Latch .....	4-29	<b>5.15</b>	<b>EEPROM (Electrically Erasable Programmable Read Only Memory) ...</b>	<b>5-20</b>	
4.13.2	D and JK Latch using CMOS Transmission Gate .....	4-30	<b>5.16</b>	<b>Flash Memory.....</b>	<b>5-22</b>	
<b>4.14</b>	<b>Static CMOS D-Flip-Flop .....</b>	<b>4-30</b>	<b>Chapter 6 : Data Path Design and System Design Issues</b>			
4.14.1	Pseudo Static D-Flip Flop.....	4-31	<b>6.1</b>	<b>Binary Adder .....</b>	<b>6-1</b>	
<b>4.15</b>	<b>T- Flip-Flop.....</b>	<b>4-32</b>	<b>6.2</b>	<b>Half Adder.....</b>	<b>6-1</b>	
<b>4.16</b>	<b>Dynamic Sequential Circuits.....</b>	<b>4-33</b>	<b>6.3</b>	<b>1-bit Full Adder.....</b>	<b>6-2</b>	
4.16.1	Dynamic Flip-Flop (1 - Bit Shift Register) .....	4-34	<b>6.4</b>	<b>Ripple Carry Adder.....</b>	<b>6-8</b>	
<b>4.17</b>	<b>D-Flip Flop using C2MOS Logic.....</b>	<b>4-35</b>	<b>6.5</b>	<b>Carry Look Ahead Adder .....</b>	<b>6-10</b>	
<b>4.18</b>	<b>Simple Shift Register.....</b>	<b>4-36</b>	<b>6.6</b>	<b>Carry Skip Adder .....</b>	<b>6-15</b>	
<b>Chapter 5 : Semiconductor Memorie</b>			<b>5.1 to 5-24</b>	<b>6.7</b>	<b>Carry Select Adder .....</b>	<b>6-18</b>
<b>5.1</b>	<b>Introduction.....</b>	<b>5-1</b>	<b>6.8</b>	<b>Carry Save Adder .....</b>	<b>6-18</b>	
<b>5.2</b>	<b>Random Access Memory (RAM).....</b>	<b>5-3</b>				
<b>5.3</b>	<b>Static RAM.....</b>	<b>5-3</b>				



<b>6.9</b>	<b>Multiplier.....</b>	<b>6-20</b>	6.19.1	Resistance.....	6-35
<b>6.10</b>	<b>Barrel Shifter.....</b>	<b>6-21</b>	6.19.2	Capacitance.....	6-36
<b>6.11</b>	<b>Timing Classification of Digital Systems.....</b>	<b>6-22</b>	<b>6.20</b>	<b>Modeling Wires.....</b>	<b>6-38</b>
<b>6.12</b>	<b>Synchronous Timing Basics .....</b>	<b>6-22</b>	6.20.1	Ideal Wire Model .....	6-38
6.12.1	Clock Skew.....	6-22	6.20.2	Lumped Model.....	6-38
6.12.2	Clock Jitter .....	6-24	6.20.3	Lumped RC Model.....	6-38
6.12.3	Combined Estimation of Clock Skew and Jitter.....	6-25	6.20.4	Distributed RC Line .....	6-43
<b>6.13</b>	<b>On Chip Clock Generation and Distribution.....</b>	<b>6-26</b>	6.20.5	Interconnect Scaling .....	6-44
6.13.1	Primary Clock Generation.....	6-26	<b>6.21</b>	<b>Charge Sharing.....</b>	<b>6-45</b>
<b>6.14</b>	<b>Clock Generators.....</b>	<b>6-27</b>	<b>6.22</b>	<b>Crosstalk .....</b>	<b>6-47</b>
<b>6.15</b>	<b>Clock Distribution.....</b>	<b>6-28</b>	<b>Chapter 7 : RTL Design</b> <b>7-1 to 7-6</b>		
<b>6.16</b>	<b>Clock Stabilization.....</b>	<b>6-29</b>	<b>7.1</b>	<b>Introduction.....</b>	<b>7-1</b>
6.16.1	Phase Locked Loop (PLL) .....	6-29	7.1.1	High Level State Machines (HLSM) .....	7-1
<b>6.17</b>	<b>Low Power CMOS Circuit.....</b>	<b>6-30</b>	<b>7.2</b>	<b>RTL Design Process .....</b>	<b>7-1</b>
<b>6.18</b>	<b>Input and Output Circuits .....</b>	<b>6-33</b>	<b>7.3</b>	<b>RTL Design of Soda Dispenser Machine .....</b>	<b>7-1</b>
<b>6.19</b>	<b>Interconnect Parameters .....</b>	<b>6-34</b>	<b>7.4</b>	<b>FIR Filter Design.....</b>	<b>7-5</b>